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| 10/728,398 | 12/05/2003 | William C. Moyer | SC13064TH | 9268 |

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| EXAMINER | |
|---|---|
| MEHRMANESH, ELMIRA | |
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| 2113 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/728,398 | MOYER ET AL. | |
| | Examiner | Art Unit | |
| | Elmira Mehrmanesh | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *11-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This action is in response to an amendment filed on February 13, 2007 for the application of Moyer et al., for "Apparatus and method for time ordering events in a system having multiple time domains" filed December 5, 2003.

Claims 11-34 are pending in the application.

Claims 11-34 are rejected under 35 USC § 103.

Claims 35-45 have been cancelled.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11-24 and 26-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards (U.S. Patent No. 6,487,683) in view of Steinberg et al. (U.S. Patent No. 6,966,015).

As per claim 11, Edwards discloses a system for time ordering events comprising: a plurality of functional circuit modules (Fig. 8) each functional circuit module (Fig. 10A, elements 200A-F) the time stamping circuitry providing a message that indicates a point in time when a predetermined event occurs (Fig. 6D, element 148)

an interface module coupled to each of the plurality of functional circuit modules, the interface module providing control information to the plurality of functional circuit modules to indicate at least one operating condition that triggers (Fig. 10B, elements 180A-F) the predetermined event, the interface module receiving at least one time stamping message from a first time domain when the predetermined event occurs (Fig. 10B, elements 112A-F) in one of a plurality of time domains including the first time domain (Fig. 6D, element 148).

Edwards fails to explicitly disclose different time domains.

Steinberg teaches:

being clocked by a clock that represents a different time domain and having time stamping circuitry (Fig. 2 and Fig. 3, element 44).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of System-on-chip debugging of Edward's in combination with the method of reducing false alarms in network fault management systems of Steinberg et al's to provide debugging information.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Edwards discloses a debugging system for System-on-chip devices (Fig. 1). Steinberg et al. discloses a method of correlating event

data in different time slices (Fig. 1).

As per claim 12, Edwards discloses the interface module further comprises: storage circuitry for storing the control information (Fig. 10B, elements 112A-F) as programmable control information that determines (col. 19, lines 22-24) the at least one operating condition that triggers the predetermined event (col. 13, lines 57-65).

As per claim 13, Edwards discloses the at least one operating condition that triggers the predetermined event further comprises at least one of: entrance into or exit from a power mode of operation, a change in source of a clock, a change in clock periodicity, a predetermined change in a hardware counter value, entry into and exit from a debug mode of operation, and occurrence of at least one user programmable event (col. 7, lines 61-67 through col. 8, lines 1-9).

As per claim 14, Edwards discloses the time stamping circuitry further comprises: a counter for determining either absolute or relative time in a corresponding functional circuit module (Fig. 6E, element 154)

time domain identification circuitry for providing a time domain identifier (Fig. 5A, elements 122, 126)

clock status circuitry for providing one or more operating characteristics of a clock in the corresponding functional circuit module (Fig. 9).

As per claim 15, Edwards discloses the time stamping circuitry further comprises circuitry for generating a code to be included in each message to identify a format of information included in a corresponding message (Fig. 6D, element 146).

As per claim 16, Edwards discloses the interface module further comprises an arbiter having circuitry for generating a code to be included in each time stamping message to identify a format of information (Fig. 6D, element 146) included in a corresponding time stamping message (Fig. 6D, element 148).

As per claim 17, Edwards discloses the message provided by at least one of the plurality of functional circuit modules (Fig. 10A) has a format that comprises at least a time count value (Fig. 6E, element 154) that is an absolute value referenced to a known starting value, status information of a clock signal associated with one of the functional circuit modules (col. 19, lines 38-46) and an identifier that indicates a corresponding time domain associated with the time stamping message (Fig. 6D, element 148).

As per claim 18, Edwards discloses the message has a format that further comprises a field that identifies that the format of the time stamping message has an absolute value time count value (Fig. 6D, element 146, 148) and (Fig. 6E, element 154).

As per claim 19, Edwards discloses the message provided by at least one of the plurality of functional circuit modules (Fig. 10A) has a format that comprises at least a

time count value (Fig. 6E, element 154) that is a relative value referenced to a last occurring predetermined event, status information of a clock signal associated with one of the functional circuit modules (col. 19, lines 38-46) and an identifier that indicates a corresponding time domain associated with the time stamping message (Fig. 6D, element 148).

As per claim 20, Edwards discloses the message has a format that further comprises a field that identifies that the format of the time stamping message having a relative value time count value (Fig. 6D, element 146, 148) and (Fig. 6E, element 154).

As per claim 21, Edwards discloses the time stamping message has a format that comprises a time count value corresponding to each of the functional circuit modules and predetermined status information associated with each of the functional circuit modules when the predetermined event occurs (Fig. 6D, element 146, 148) and (Fig. 6E, element 154).

As per claim 22, Edwards discloses the control information is programmable (col. 19, lines 22-24).

As per claim 23, Edwards discloses the interface module further comprises: at least one register for storing the control information (Fig. 10B, elements 112A-F).

As per claim 24, Edwards discloses the interface module provides time stamping messages from all time domains at a common interface port (Fig. 10A).

As per claim 26, Edwards discloses a system for time ordering events comprising: a plurality of functional circuit module (Fig. 8) means, the time stamping circuit means providing a message that indicates a point in time when a predetermined event occurs (Fig. 6D, element 148)

interface module means coupled to each of the plurality of functional circuit module means (Fig. 10B, elements 180A-F) the interface module means providing control information to the plurality of functional circuit module means to indicate at least one operating condition that triggers the predetermined event (Fig. 10B, elements 180A-F) the interface module means receiving at least one time stamping message from a first time domain when the predetermined event occurs (Fig. 10B, elements 112A-F) in one of a plurality of time domains including the first time domain (Fig. 6D, element 148).

Edwards fails to explicitly disclose different time domains.

Steinberg teaches:

being clocked by a clock that represents a different time domain and having time stamping circuitry (Fig. 2 and Fig. 3, element 44).

As per claim 27, Edwards discloses the time stamping messages from all time domains are provided by interface module means at a common interface port means (Fig. 10A).

As per claim 28, Edwards discloses a system comprising: a plurality of functional circuit modules (Fig. 8 and 10A-B) on a same integrated circuit (col. 4, lines 16-18), each functional circuit module being clocked by a clock (Fig. 9, element 205) and each functional module having time stamping circuitry operating at independent clock rates for providing timestamp messages (Fig. 6D, element 148).

Edwards fails to explicitly disclose different time domains.

Steinberg teaches:

being clocked by a clock that represents a different time domain and having time stamping circuitry (Fig. 2 and Fig. 3, element 44).

As per claim 29, Edwards discloses the timestamp messages each indicate a point in time when a predetermined event occurs (Fig. 6D, element 148).

As per claim 30, Edwards discloses an interface module coupled to each of the plurality of functional circuit modules (Fig. 10B, elements 180A-F) the interface module providing control information to the plurality of functional circuit modules to indicate at least one operating condition that triggers the predetermined event (Fig. 10B, elements 180A-F) the interface module receiving at least one time stamping message (Fig. 6D, element 148) from a first time domain when the predetermined event occurs in one of a plurality of time domains including the first time domain (Fig. 6E, element 156).

As per claim 31, Edwards discloses a method of reconstructing time ordering of events that occur in multiple time domains in a system, the method comprising: receiving multiple time stamping messages (Fig. 6D, element 148) in one of an ordered time sequence and an unordered time sequence; tracking relative count values of multiple time domain counters (Fig. 5B, element 126) and (Fig. 6E, element 156) and (Fig. 6F, element 158) associated with the multiple time domains and operating at independent clock rates; and sorting debug information in time ordered sequence, the debug information being associated with a timestamp (Fig. 6D, element 148).

Edwards fails to explicitly disclose different time domains.

Steinberg teaches:

A timestamp provided from one of the multiple time domains (Fig. 2 and Fig. 3, element 44).

As per claim 32, Edwards discloses providing the debug information via a debug message (Fig. 3, elements 72, 32).

As per claim 33, Edwards discloses implementing the debug messages as at least one of a program trace message, a data trace message and a watchpoint message (Fig. 3) and (col. 14, lines 34-52).

As per claim 34, Edwards discloses generating the multiple timestamp messages (Fig. 6D, element 148) by: providing control information corresponding to each of

multiple time domains (Fig. 6C, 6D), the control information indicating when a timestamp message for each of the multiple time domains is to be generated (Fig. 6D, element 148) determining when a time domain event that requires generation of a timestamp message occurs in any one of the multiple time domains (Fig. 6E, element 154) and generating a timestamp message corresponding to a predetermined one of the multiple time domains in response to determining that the time domain event occurred (Fig. 6D, element 148).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards (U.S. Patent No. 6,487,683) in view of Steinberg et al. (U.S. Patent No. 6,966,015) and in further view of Rohfleisch et al. (U.S. Patent No. 7,058,855).

As per claim 25, Edwards in view of Steinberg fails to explicitly disclose IEEE ISTO 5001 (NEXUS).

Rohfleisch teaches:

the common interface port of the interface module meets IEEE ISTO 5001 (NEXUS) compliance (col. 7, lines 65-67 through col. 8, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of System-on-chip debugging of Edward's in combination with the on-chip debugging system of Rohfleisch et al. to provide debugging information.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Edwards discloses a debugging system for System-on-chip devices (Fig. 1). Rohfleisch et al. teaches of the on-chip debugging system of integrated circuit (Fig. 1) and (col. 7, lines 60-65). Edwards uses the method of generating timestamp messages to identify events (Fig. 6D, element 148). Rohfleisch et al. also discloses a method of using timestamps (col. 8, lines 9-22).

***Response to Arguments***

Applicant's arguments filed February 13, 2007 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both of Edwards and Steinberg inventions are directed toward detecting faults in hardware devices (Edwards, Fig. 1 and col. 13, lines 19-22) and (Steinberg, Fig. 1 and col. 4, lines 51-53) in which the system monitors a plurality of functional circuit modules (Edwards, Fig. 10A, elements 200A-F) and (Steinberg, Fig. 1, element 16 and col. 4, lines 61-62) at different times. Edwards discloses multiple clock cycles (col. 18, lines 28-31, next clock

cycle) and Steinberg discloses multiple discrete time periods (col. 6, lines 53-55) with time stamping circuitry (Edwards, Fig. 6D, element 148) and (Steinberg, col. 8, lines 6-9). Edwards further discloses that in view of his invention various alterations, modifications, and improvements will readily occur to those skilled in the art (col. 21, lines 65-67). Steinberg discloses monitoring devices over a window of time provides improved diagnosis of a complex problem (col. 3, lines 1-10). Steinberg's fault monitoring system is a modification of Edwards debugging system by applying continuous monitoring over a plurality of time slices.

Applicant argues that Steinberg et al. does not teach or suggest a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain and having time stamping circuitry, the time stamping circuitry providing a message that indicates a point in time when a predetermined event occurs. The Examiner respectfully disagrees and would like to point out that on page 3 of the previous office Action mailed on December 11, 2006, Steinberg et al. was cited for the claimed limitation of "a clock that represents a different time domain and having time stamping circuitry". Steinberg's figure 1 shows a system for detecting faults in a network. Monitored network devices 16 include many types of **hardware devices such as CPUs**, routers, printers, network interface card, ect. (col. 4, lines 61-62). These monitored devices are interpreted as a plurality of functional circuit modules. Steinberg et al. further discloses monitoring these devices over multiple discrete time periods. Noting col. 6, lines 53-55, wherein Steinberg discloses ... the transitions of the indicator states over **multiple discrete time periods** for the monitored

indicators, step 44. This analysis reveals the extent of coincidence of transitions of indicators during each time period. Steinberg discloses monitoring indicators and their transitions over multiple discrete time periods by issuing a timestamp for each indication over the specific time period (noting col. 8, lines 6-9, wherein Steinberg discloses, if they have changed in the same direction in the past 5 seconds from the **timestamp** of the most recently changed indicator). Therefore, the disclosed monitoring of the hardware devices (*i.e. plurality of functional circuit modules*) over multiple discrete time periods (*i.e. each functional circuit being clocked by a clock that represents a different time domain*) and indicators changed from the timestamp of the most recently changed (*i.e. having time stamping circuitry*) reads on the claimed limitation of "a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain and having time stamping circuitry".

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1 .136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1 .136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 9-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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